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Design of Low Power Double Edge Triggered Comparator for Successive Approximation Register (SAR) ADC

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Abstract: High speed analog to digital converters (ADC), sense amplifiers, RFID applications, data receivers with low power and area efficient designs has appealed a wide variety of dynamic comparators. This paper presents design of low power double edge triggered comparator for successive approximation register (SAR) ADC. In this paper a low power double edge triggered comparator is designed for an area efficient and double edge triggered operation for a small delay. The proposed comparator structure consists of a separate cross coupled and input stage for enabling a fast operation over a wide range of common mode and supply voltages. The proposed method has been designed and simulated by using 130nm CMOS technology. The results indicate that in the proposed double edge triggered comparator, area and power consumption are significantly reduced and achieves the high speed of operation.

Keywords: comparator, ADC's, double edge triggered, SAR.

I. INTRODUCTION

The fundamental function of a CMOS comparator is to determine whether a signal is greater or smaller than zero. It can also be used to produce a binary signal by comparing the input signal and reference signal. A double-tail sense amplifier [11] which uses one tail for the input stage and another tail for the latching stage. These types of amplifiers can operate at minimal supply voltages as less stacking is needed in this topology. Compared to other works [4, 7, and 9] the average power consumption is high. The clocked comparator [9] comprises of the regenerative and amplification stages, implemented using 10 MOS transistors. The area and delay is reduced compared to the sense amplifier [11]. A reconfigurable low- noise dynamic comparator [4] reduces the input referred noise almost by half. This result in a better output driving capability. The control of the noise, offset and power consumption can be carried out by a simply reconfigured clock delay [7, 9]. The comparator uses multiple clock delays along with the first and second stages to attain reconfigurable capability. The area and the power consumption of such a comparator were high when compared to all related works [9, 10, and 11]. The delay is significantly reduced compared to [11, 2]. Single stage comparator [5], achieved the fastest comparison speed with lowest power dissipation compared to the conventional dynamic comparators. Static power of the transistors got reduced. The area also got reduced compared to [12]. [13].

Comparators play a key role in modern mixed signal systems. For high speed applications such as data links, on-chip high frequency signal testing, analog-to- digital converters and sense amplifiers, two important features viz., speed and resolution are required. Between power supply and ground the regenerative stage can be designed to start its operation, if priority is given to speed of the comparator. An example is a pre-amplifier based clocked comparator [2]. However in the mentioned case the static power consumption remains relatively higher. If power reduction is given priority, the number of transistors increases thereby reducing the delay as in a double tail latched comparator [1]. This paper presents a detailed analysis on the power consumption, area and delay for various architectures of conventional dynamic comparators. Furthermore a new dynamic comparator which does not require too many transistors stacking or voltage boost based on the double edge triggered structure is proposed. It is found that mere removal of a few minimum-size transistors from the conventional dynamic comparator profoundly reduces power consumption and area. This modification also resulted in reducing considerable amount of delay while compared to the conventional comparators. The proposed work deals with increasing the speed of conversion for an 8-bit SAR ADC. In the paper the sections are categorized as follows: Section II describes the working of proposed double edge triggered comparator and proposed comparator performance, Section III discusses the overall architecture of low power, high speed SAR ADC and discusses the simulation results of SAR ADC and comparison with other proposed architectures while Section IV concludes the paper.

II. PROPOSED DOUBLE EDGE TRIGGERED COMPARATOR

The double edge triggered architecture implies a better performance in applications which require a low voltage. Hence in our work too, such architecture was used to design the comparator. The major goal of the proposed

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comparator is to increase ΔVfn/fp there by reducing the area. It is a single stage comparator. The proposed comparator is shown in figure 1. Number of transistors and power dissipation is reduced by the use of a single stage operation. Initially the design of the cross coupled inverter pair is carried out in a separate manner. The CMOS inverter transistor sizing rule states that the PMOS size should always be equal to three times the size of NMOS. This condition is strictly followed. Next the optimization of these transistor sizes is carried out. This is done in order to keep the DC biasing at a level which is somewhat higher than the supply voltage midpoint. It should be noted that the transistor widths were kept around 180 nm to enhance speed in this digital design. The transistor sizes were adjusted such that the circuit remains self-biased. The values are compared by using the cross coupled inverters NMOS 1&2, PMOS1&2 transistors. The cross coupled inverter is also used to store the values. Switching NMOS transistors NMOS3& NMOS4 is connected to the differential output nodes of the comparator. The proposed comparator operates in the following way. One comparison cycle of the comparator consists of the reset and regeneration phase. During the reset phase, the gates of the transistors NMOS3 and NMOS4 receive zero as the input. In the regeneration phase, the gates of the transistor NMOS3 and NMOS4 receive VCC as the input.

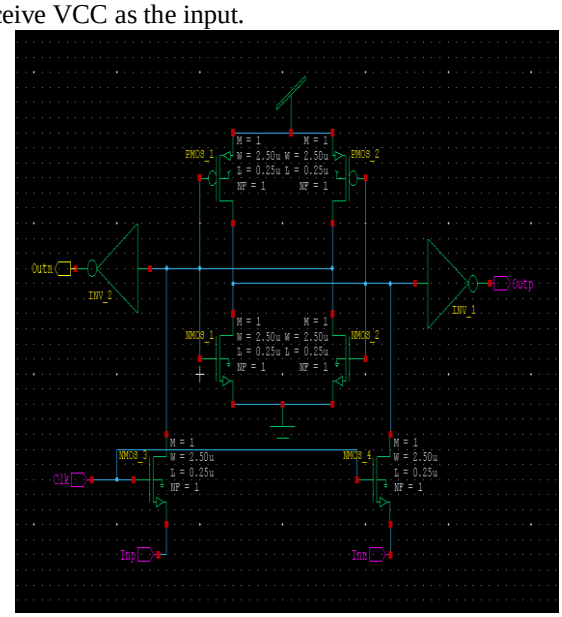

Fig 1: Schematic of Proposed Double Edge Triggered Comparator

A. Reset Phase

The duration between the states of high clock to low clock refers to the reset phase. In the reset phase NMOS3 and NMOS4 turns on thereby connecting the pre-amplifier output to the inverter node differential ports. These inverters are in turn used to generate the output.

B. Regeneration Phase

The starting of the regeneration phase is indicated by the transition of the clock from low to high. In the regeneration phase NMOS3 and NMOS4 turns off. At the same time, depending on the charge imbalance generated due to the input signal difference, the inverter pair moves either the outn or outp node to VCC or GND.

Figure 2 shows the simulation results of the proposed comparator. The design of the circuit was done using 180nm technology and simulated by W-Edit. From the simulation result, the power consumption is reduced when compared to other related works. The area of the comparator also got reduced. From figureB6 we can see that, the comparator starts to work when the clock is high and gives the output at falling edge. The comparison of the comparator waveforms can be explained as follows. If the comparator input is higher than the reference voltage, Vref, then the output will be a logical "1" function. On the other hand when the comparator input is lower than the reference voltage Vref then the output will be a logical "0" function. The waveforms are shown in figure 2. They are the efficient mandatory functions, which are generated by the comparator.

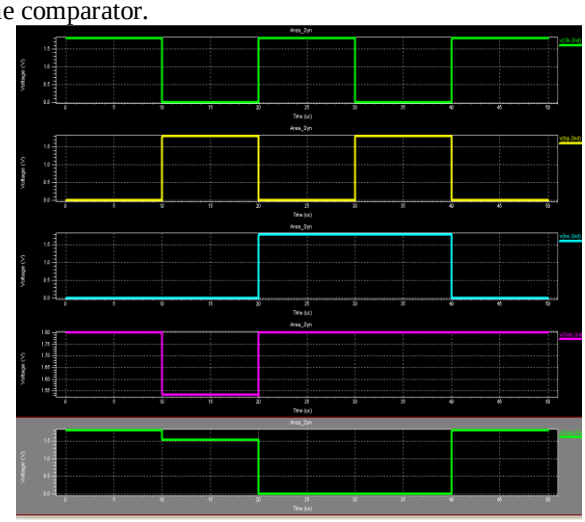

Fig 2: Simulation Result of Proposed Comparator

III. LOW POWER SAR ADC

Figure 3 shows the circuit diagram of the complete low power 8-bit SAR ADC design using proposed comparator to trigger and complete the process of conversion in a faster mode.

The comprehensive working can be summarized as the comparator outputs being connected to a NOR circuitry which will be used as a ready pulse (clock) to be used by the SAR. By this approach we avoid an external clock required by the SAR. As a preset condition the SAR register is set to a mid-value range based on the resolution (N=Number of bits) of the ADC.

The SAR logic will now trigger and shift to the correct logic levels based on the clock signal provided by the NOR circuitry. The operation of the comparator is as follows; when the comparator output =0, the shift registers will reset. When the output=1, the shift register output will be 10000000.depending on the comparator output the conversion will takes place.

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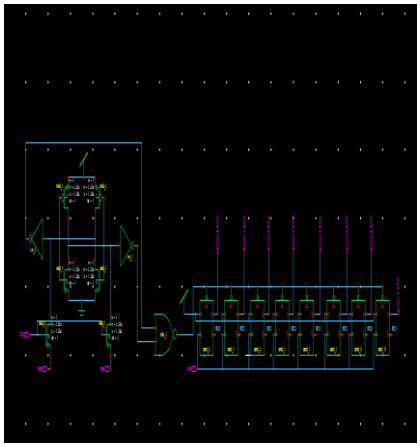

Fig 3: Architecture of the complete low power 8-bit SAR ADC

A. Simulation Result

Figure 4 presents the simulation result of 8-bit SAR ADC with proposed double edge triggered comparator. As shown in the Figure 4, the proposed design achieves a faster level of conversion process in comparison with other works. After 8 ready signals generated by the comparator output, all the individual bits in the SAR register attain the correct logic levels. The design of the circuit was done using 180nm technology and simulated by W-Edit.From the simulation result,the power consumption is reduced when compared to other related works.The area of the comparator also got reduced.

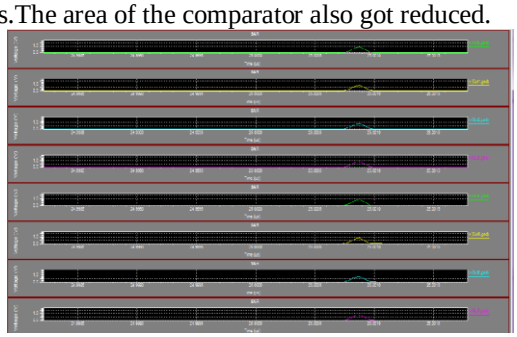

Fig 4: Simulation Result of 8-Bit SAR ADC with Proposed Double Edge Triggered Comparator

B. Comparison with Other Works

Parameters	Dual-Tail sense amplifier	Clocked Comparator	Reconfigurable Low-Noise Dynamic Comparator	Single stage comparator	Proposed comparator
Average power consumption	0.746µw	0.646 µw	0.59µw	0.1903 µw	0.106µw
Static power	2.23µw	1.9447µw	1.9335µw	1.0903 µw	1.82 µw
Power delay product(PDP)	66.9nws	77.6nws	7.72nws	3.27nws	7.28 nws
Number of transistor	12	12	17	13	10
Static current	1.238µA	1.08µA	1.07µA	0.605 µA	1.011µA

Table 1: Performance Comparison of Comparators

Table 1 shows the performance comparison of the comparators. From that, the proposed double edge triggered comparator reduces the average power consumption and increases its speed. Table 2 shows the performance comparison of the SAR ADC with different comparators.

Parameters	Dual-Tail sense amplifier	Clocked Comparator	Reconfigurable Low-Noise Dynamic Comparator	Single stage comparator	Proposed comparator
Average power consumption	0.72µw	0.52 µw	0.44µw	0.34 µw	0.26µw
Static power	3.87µw	1.329µw	1.378µw	1.31 µw	1.34µw
Power delay product(PDP)	38.7nws	5.316nws	4.825nws	3.14nws	4.68nws
Static current	2.15µA	0.738µA	0.765 µA	0.691 µA	0.744µA

Table2: Performance Comparison of SAR ADC with Comparator

IV. CONCLUSION

A low power, small area and high speed double edge triggered comparator has been proposed. The comparator does not require boosted voltage or stacking of too many transistors. Measured result show that average power consumption is 0.106µw which is better than what is obtained with the comparing architectures. This results in improved process of comparison and it also accelerated conversion process of the ADC. The delay of the comparator is higher than [5] but not more than [11, 9, and 4].considering the overall performance of the comparator it is more efficient than the others. The simulation results confirm the entire 8-bit conversion process to be completed in 75ns with a total power dissipation of 47.18µW.

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